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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/591,680	HERBORDT ET AL.	
	Examiner	Art Unit	
	RYAN COYER	2197	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *2,4-14,16,21-25,27,28,30,36,37,39,40,42,44,46,47,49-51,53,54 and 56-60* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 2,4-14,16,21-25,27,28,30,36,37,39,40,42,44,46,47,49-51,53,54 and 56-60.

DETAILED ACTION

This is in response to the amendment to Application 10/591680, filed on 10/26/2011, in which claims 2, 4-14, 16, 21-25, 27, 28, 30, 36, 37, 39, 40, 42, 44, 46, 47, 49-51, 53, 54 and 56-60 are presented for examination. Claims 1, 3, 15, 17-20, 26, 29, 31-35, 38, 41, 43, 45, 48, 52, and 55 are canceled by the amendment. Of the remaining claims, 2, 8, 16, 21, and 30 are in independent form.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 2, 4-14, 16, 21-25, 27, 28, 30, 36, 37, 39, 40, 42, 44, 46, 47, 49-51, 53, 54 and 56-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ussery et al., USPAT 6,484,304, hereinafter "Ussery," in view of Shackleford et al., USPAT 5,896,521, hereinafter "Shackleford." Claims 2, 4-7, 21-25, 27-28, 30, 46-47, 49-51, 53-

54, and 56-60 properly recite "means plus function" language and will be interpreted in accordance with 35 U.S.C. 112, sixth paragraph. Examiner asserts that the specification does not preclude the interpretations of claims 2, 4-7, 21-25, 27-28, 30, 46-47, 49-51, 53-54, and 56-60 employed in the following rejections.

Regarding claim 2, Ussery discloses **"[a]n application specific coprocessor system** (see, e.g., fig. 2. sec. 54; col. 4 ln. 17-22, col. 5 ln. 20-23; "loads the program image 60 into the PSA IC 54. This loads the binary program image into on-chip program memory on the PSA IC.") **for use with a processor for use in massive data manipulations specific to an application and adapted for attachment to a workstation having a general purpose processor,** (see, e.g., fig. 2 sec. 62, 64; col. 5 ln. 5-23; "The PSA analysis system 62 is a graphical analysis environment that allows the user to analyze certain characteristics of their application running on a target PSA IC"; "A PSA Image Loader/Programmer 64 loads the program image 60 into the PSA IC 54. This loads the binary program image into on-chip program memory on the PSA IC.") **said coprocessor system having programming code which is assembled as instructions for said specific application in combination with accelerator environment specific requirements, independently provided."** (see. e.g., fig. 2 sec. 52, 56, 58, 60; col. 4 ln. 23-30, 64-67; col. 5 ln. 1-4, 20-30; "The user program 56 containing the custom code that defines the system specification for the ASIC and the application libraries 58 is parsed by the PSA Compiler 52. The PSA compiler 52 converts the user program 56 into a program image 60 of the system specifications for

the ASIC that comprises a series of microtasks. Each microtask is a Very Long Instruction Word (VLIW) program for a target task engine in the PSA IC 54.") **wherein said environment specific instructions are accessed by a compiler in response to user input in an application specific form;** (see, e.g., fig. 3 and associated text; col. 4 ln. 64 – col. 5 ln. 4; "The PSA compiler 52 converts the user program 56 into a program image 60 of the system specifications for the ASIC that comprises a series of microtasks.") **and wherein said compiler comprises:**

a user interface to permit an application trained non circuit design trained user to enter instructions to achieve application specific accelerated processing; (col. 5 ln. 5-20; "graphical analysis environment that allows the user to analyze certain characteristics of their application running on a target PSA IC."; col. 4 ln. 55-58; "reduces the design cycle time and the level of skill required to produce the custom integrated circuit.")

means for creating an internal representation reflecting the operational characteristics of a coprocessor corresponding to application specific accelerated processing needs; (see, e.g., col. 5 ln. 5-20; "The PSA simulator is a software model of a specific configuration of the PSA IC hardware that can execute the program image 60 produced by the PSA compiler 52").

Ussery does not explicitly disclose the limitation further comprising **"means for identifying bit demands for the application specific accelerated processing needs such that each intermediate step in a calculation is allocated a minimal number of bits necessary for producing a final result that fulfills domain-specific**

objectives." However, Shackleford discloses the aforementioned limitation at col. 3, ln. 47-51; col. 6 ln. 50-53 ("processor synthesis system . . . which can reduce the number of software development steps specifically adapted to the processor architecture to be synthesized" wherein "the CPU bit width is customized to the requirement of [an] application."). In other words, Shackleford identifies the minimum bit width required for an application with a view toward synthesizing an application specific integrated circuit (ASIC) that is optimized for the application. As noted in the Response to Arguments section, "each intermediate step" may be allocated the same bit width, which is the "minimal number of bits necessary for producing a final result that fulfills domain-specific objectives." Alternatively, even if "each intermediate step" could be allocated a different bit width, which is *not* clearly supported by the specification, the structure of the aforementioned claim limitation does not require any variation in allocation.

Ussery and Shackleford are directed toward the fields of processor synthesis (also known as generating ASICs) and therefore are analogous art. At the time of the invention, it would have appeared obvious to one of ordinary skill in the art to enhance the processor synthesis method of Ussery by incorporating the bit-width analysis method of Shackleford. A source of motiviation would have been to ensure that "maximum cost efficiency is obtained." (Shackleford, col. 6 ln. 52-53). The result of combining Shackleford and Ussery would be both predictable and useful: the minimum processor bit-width would be used, thereby reducing development costs. Therefore, the instant claim is unpatentable over Ussery in view of Shackleford.

Regarding claim 4, Ussery, in view of Shackleford, obviates **"[t]he coprocessor of claim 2 wherein said compiler comprises one or more of: mapper means for identifying resources available and needed for the coprocessor to provide application specific accelerated processing,** (see, e.g., Ussery col. 5 ln. 54-62, col. 6 ln. 4-14, col. 7 ln. 3-13; user-defined functions are mapped to target task engines and then optimized) **balancing means for identifying the step by step hardware needs of the coprocessor for the application specific acceleration."** (see, e.g., Ussery col. 6 ln. 4-14; "The global analyzer 106 determines the optimal task engines on which to execute the functionality of a given task. This is done by analyzing the required operations of the task (addition, multiplication, etc.) and matching those to a task engine that can optimally support the collection of operations required by the task.").

Regarding claim 5, Ussery, in view of Shackleford, obviates **"[t]he coprocessor of claim 4 wherein said mapper means accepts as input domain-specific policy information, estimates of the amount of logic needed for each processing element, and hardware context information that states what amounts of each logic resource exist on a given coprocessor to enable the largest possible number of processing elements said coprocessor can support."** (see, e.g., Ussery col. 5 ln. 54-62, col. 6 ln. 4-14, col. 7 ln. 3-13; user-defined functions are mapped to target task engines and then optimized).

Regarding claim 6, Ussery, in view of Shackleford, obviates **"[t]he coprocessor of claim 5 wherein said balancing means analyzes the processing speed of said coprocessor at each step and allocates parallel hardware in proportion to a speed**

requirement." (see, e.g., Ussery col. 7 ln. 3-13; "The microtask analyzer and code generator 110 optimizes the microtasks for parallelism if multiple computation units are in the target task engine. Rather than executing each operation in sequence, the microtask analyzer and code generator 110 determines operations which can be executed independent of each other and allocates these operations to different computation units.").

Regarding claim 7, Ussery, in view of Shackleford, obviates **"[t]he coprocessor of claim 2, wherein said compiler further comprises one or more of: prerecorded information reflecting the programming requirements for a general area of applications; programming content which reflects application requirements and hardware characteristics; and coprocessor specific hardware availability."** (see, e.g., Ussery col. 6 ln. 4-14; application requirements are evaluated and mapped to appropriate task engines comprising the necessary processing power.).

Regarding claim 8, Ussery discloses **"[a] method for programming an accelerating coprocessor** (see, e.g., fig. 2. Sec. 54; col. 4 ln. 17-22, col. 5 ln. 20-23; "loads the program image 60 into the PSA IC 54. This loads the binary program image into on-chip program memory on the PSA IC.") **comprising the steps of: accessing data reflective of programming requirements for a general area of applications;** (see, e.g,. fig. 2 and associated text; col. 4 ln. 23-30; "To generate the ASIC using the method of the present invention, an end user (not shown) develops a user program 56 that includes custom code which defines the system specification for the ASIC. The user program 56 may incorporate application libraries 58 of verified code that perform

certain predetermined functions likely to be found in target application. These application libraries 58 are essentially virtual intellectual property ("Virtual IP") blocks.")

Ussery does not explicitly disclose the limitation further comprising **"identifying bit demands for the accelerating coprocessor acceleration function such that each intermediate step in a calculation is allocated a minimal number of bits necessary for producing a final result that fulfills domain-specific objectives."** However, Shackleford discloses the aforementioned limitation at col. 3, ln. 47-51; col. 6 ln. 50-53 ("processor synthesis system . . . which can reduce the number of software development steps specifically adapted to the processor architecture to be synthesized" wherein "the CPU bit width is customized to the requirement of [an] application."). In other words, Shackleford identifies the minimum bit width required for an application with a view toward synthesizing an application specific integrated circuit (ASIC) that is optimized for the application. As noted in the Response to Arguments section, "each intermediate step" may be allocated the same bit width, which is the "minimal number of bits necessary for producing a final result that fulfills domain-specific objectives." Alternatively, even if "each intermediate step" could be allocated a different bit width, which is *not* clearly supported by the specification, the structure of the aforementioned claim limitation does not require any variation in allocation.

Ussery and Shackleford are directed toward the fields of processor synthesis (also known as generating ASICs) and therefore are analogous art. At the time of the invention, it would have appeared obvious to one of ordinary skill in the art to enhance the processor synthesis method of Ussery by incorporating the bit-width analysis

method of Shackleford. A source of motiviation would have been to ensure that "maximum cost efficiency is obtained." (Shackleford, col. 6 ln. 52-53). The result of combining Shackleford and Ussery would be both predictable and useful: the minimum processor bit-width would be used, thereby reducing development costs. Therefore, the instant claim is unpatentable over Ussery in view of Shackleford.

Regarding claim 9, Ussery, in view of Shackleford, obviates **"[t]he method for programming an accelerating coprocessor of claim 8 comprising the step of: accessing data reflective of programming content which reflects application requirements and hardware characteristics."** (see, e.g., Ussery fig. 3 and associated text; col. 4 ln. 64 – col. 5 ln. 4; "The PSA compiler 52 converts the user program 56 into a program image 60 of the system specifications for the ASIC that comprises a series of microtasks.").

Regarding claim 10, Ussery, in view of Shackleford, obviates **"[t]he method for programming an accelerating coprocessor of claim 8 comprising the step of: accessing data reflective of coprocessor specific hardware availability."** (see, e.g., Ussery col. 7 ln. 3-13; "The microtask analyzer and code generator 110 optimizes the microtasks for parallelism if multiple computation units are in the target task engine. Rather than executing each operation in sequence, the microtask analyzer and code generator 110 determines operations which can be executed independent of each other and allocates these operations to different computation units.").

Regarding claim 11, Ussery, in view of Shackleford, obviates **"[t]he method of claim 8 further comprising the step of: permitting an application trained non**

circuit design trained user to enter instructions to achieve accelerated performance." (see, e.g., col. 4 ln. 56-63; col. 5 ln. 5-20; "graphical analysis environment that allows the user to analyze certain characteristics of their application running on a target PSA IC."; col. 4 ln. 55-58; "reduces the design cycle time and the level of skill required to produce the custom integrated circuit.").

Regarding claim 12, Ussery, in view of Shackleford, obviates **"[t]he method of claim 8 further comprising the step of: creating an internal representation reflecting the operational characteristics of a coprocessor corresponding to application specific accelerated processing needs."** (see, e.g., Ussery col. 5 ln. 5-20; "The PSA simulator is a software model of a specific configuration of the PSA IC hardware that can execute the program image 60 produced by the PSA compiler 52").

Regarding claim 13, Ussery, in view of Shackleford, obviates **"[t]he method of claim 8 further comprising the step of: identifying resources available and needed for the coprocessor to provide application specific accelerated processing."** (see, e.g., Ussery col. 5 ln. 54-62, col. 6 ln. 4-14, col. 7 ln. 3-13; user-defined functions are mapped to target task engines and then optimized; "The global analyzer 106 determines the optimal task engines on which to execute the functionality of a given task. This is done by analyzing the required operations of the task (addition, multiplication, etc.) and matching those to a task engine that can optimally support the collection of operations required by the task.").

Regarding claim 14, Ussery, in view of Shackleford, obviates **"[t]he method of claim 8 further comprising the step of: identifying the step by step hardware**

needs of the coprocessor for the application specific acceleration." (see, e.g., Ussery col. 6 ln. 4-14; "The global analyzer 106 determines the optimal task engines on which to execute the functionality of a given task. This is done by analyzing the required operations of the task (addition, multiplication, etc.) and matching those to a task engine that can optimally support the collection of operations required by the task.").

Regarding claim 16, Ussery discloses "[a] method of compiling data for **programming an accelerating coprocessor** (see, e.g., fig. 2. Sec. 54; col. 4 ln. 17-22, col. 5 ln. 20-23; "loads the program image 60 into the PSA IC 54. This loads the binary program image into on-chip program memory on the PSA IC.") **comprising the steps of: creating an internal representation reflecting the operational characteristics of a coprocessor corresponding to application specific accelerated processing needs."** (see, e.g., col. 5 ln. 5-20; "The PSA simulator is a software model of a specific configuration of the PSA IC hardware that can execute the program image 60 produced by the PSA compiler 52").

Ussery does not explicitly disclose the limitation further comprising "**identifying bit demands for the application specific coprocessor acceleration function such that each intermediate step in a calculation is allocated a minimal number of bits necessary for producing a final result that fulfills domain-specific objectives."** However, Shackleford discloses the aforementioned limitation at col. 3, ln. 47-51; col. 6 ln. 50-53 ("processor synthesis system . . . which can reduce the number of software development steps specifically adapted to the processor architecture to be synthesized" wherein "the CPU bit width is customized to the requirement of [an] application."). In

other words, Shackleford identifies the minimum bit width required for an application with a view toward synthesizing an application specific integrated circuit (ASIC) that is optimized for the application. As noted in the Response to Arguments section, "each intermediate step" may be allocated the same bit width, which is the "minimal number of bits necessary for producing a final result that fulfills domain-specific objectives." Alternatively, even if "each intermediate step" could be allocated a different bit width, which is *not* clearly supported by the specification, the structure of the aforementioned claim limitation does not require any variation in allocation.

Ussery and Shackleford are directed toward the fields of processor synthesis (also known as generating ASICs) and therefore are analogous art. At the time of the invention, it would have appeared obvious to one of ordinary skill in the art to enhance the processor synthesis method of Ussery by incorporating the bit-width analysis method of Shackleford. A source of motiviation would have been to ensure that "maximum cost efficiency is obtained." (Shackleford, col. 6 ln. 52-53). The result of combining Shackleford and Ussery would be both predictable and useful: the minimum processor bit-width would be used, thereby reducing development costs. Therefore, the instant claim is unpatentable over Ussery in view of Shackleford.

Regarding claim 36, Ussery, in view of Shackleford, obviates **"[t]he method of claim 10 further comprising the step of: permitting an application trained non circuit design trained user to enter instructions to achieve accelerated performance."** (see, e.g., Ussery col. 4 ln. 56-63; col. 5 ln. 5-20; "graphical analysis environment that allows the user to analyze certain characteristics of their application

running on a target PSA IC."; col. 4 ln. 55-58; "reduces the design cycle time and the level of skill required to produce the custom integrated circuit.").

Regarding claim 37, Ussery, in view of Shackleford, obviates **"[t]he method of claim 36 further comprising the step of: creating an internal representation reflecting the operational characteristics of a coprocessor corresponding to application specific accelerated processing needs."** (see, e.g., Ussery col. 5 ln. 5-20; "The PSA simulator is a software model of a specific configuration of the PSA IC hardware that can execute the program image 60 produced by the PSA compiler 52").

Regarding claim 39, Ussery, in view of Shackleford, obviates **"[t]he method of claim 37 further comprising the step of: identifying the step by step hardware needs of the coprocessor for the application specific acceleration."** (see, e.g., Ussery col. 7 ln. 3-13; "The microtask analyzer and code generator 110 optimizes the microtasks for parallelism if multiple computation units are in the target task engine. Rather than executing each operation in sequence, the microtask analyzer and code generator 110 determines operations which can be executed independent of each other and allocates these operations to different computation units.").

Regarding claim 40, Ussery, in view of Shackleford, obviates **"[t]he method of claim 11 further comprising the steps of: creating an internal representation reflecting the operational characteristics of a coprocessor corresponding to application specific accelerated processing needs."** (see, e.g., Ussery col. 5 ln. 5-20; "The PSA simulator is a software model of a specific configuration of the PSA IC hardware that can execute the program image 60 produced by the PSA compiler 52").

Regarding claim 42, Ussery, in view of Shackleford, obviates **"[t]he method of claim 40 further comprising the step of: identifying the step by step hardware needs of the coprocessor for the application specific acceleration."** (see, e.g., Ussery col. 7 ln. 3-13; "The microtask analyzer and code generator 110 optimizes the microtasks for parallelism if multiple computation units are in the target task engine. Rather than executing each operation in sequence, the microtask analyzer and code generator 110 determines operations which can be executed independent of each other and allocates these operations to different computation units.").

Regarding claim 44, Ussery, in view of Shackleford, obviates **"[t]he method of claim 12 further comprising the steps of: identifying the step by step hardware needs of the coprocessor for the application specific acceleration."** (see, e.g., Ussery col. 7 ln. 3-13; "The microtask analyzer and code generator 110 optimizes the microtasks for parallelism if multiple computation units are in the target task engine. Rather than executing each operation in sequence, the microtask analyzer and code generator 110 determines operations which can be executed independent of each other and allocates these operations to different computation units.").

Regarding claims 21-25, 27-28, 30, 46-47, 49-51, 53-54, and 56-57, the scope of the instant claims does not differ substantially from that of claims 8-14, 16, 36-37, 39-40, and 42. Accordingly, the rejections of claims 8-12 apply, *mutatis mutandis*, to claims 21-25; the rejections of claims 14 and 16 apply, *mutatis mutandis*, to claims 28 and 30; the rejections of claim 36-37 apply, *mutatis mutandis*, to claims 46-47; the rejection of claim 40 applies, *mutatis mutandis*, to claim 51; the rejection of claim 13 applies,

mutatis mutandis, to claims 27, 49, 53, and 56; the rejection of claim 39 applies, *mutatis mutandis*, to claim 50; and the rejection of claim 42 applies, *mutatis mutandis*, to claims 54 and 57.

Regarding claim 58, Ussery, in view of Shackleford, obviates **"[t]he compiler of claim 21 further comprising means for identifying resources available and needed for the coprocessor to provide application specific accelerated processing."** (see, e.g., Ussery col. 7 ln. 3-13; "The microtask analyzer and code generator 110 optimizes the microtasks for parallelism if multiple computation units are in the target task engine. Rather than executing each operation in sequence, the microtask analyzer and code generator 110 determines operations which can be executed independent of each other and allocates these operations to different computation units.").

Regarding claim 59, Ussery, in view of Shackleford, obviates **"[t]he compiler of claim 58 further comprising: means for identifying the step by step hardware needs of the coprocessor for the application specific acceleration."** (see, e.g., Ussery col. 7 ln. 3-13; "The microtask analyzer and code generator 110 optimizes the microtasks for parallelism if multiple computation units are in the target task engine. Rather than executing each operation in sequence, the microtask analyzer and code generator 110 determines operations which can be executed independent of each other and allocates these operations to different computation units.").

Regarding claim 60, Ussery, in view of Shackleford, obviates **"[t]he compiler of claim 27 further comprising: means for identifying the step by step hardware needs of the coprocessor for the application specific acceleration."** (see, e.g.,

Ussery col. 7 ln. 3-13; "The microtask analyzer and code generator 110 optimizes the microtasks for parallelism if multiple computation units are in the target task engine. Rather than executing each operation in sequence, the microtask analyzer and code generator 110 determines operations which can be executed independent of each other and allocates these operations to different computation units.").

Response to Arguments

Applicant's amendments to and cancellations of the claims and amendments to the specification have overcome all standing objections and rejections. However, Applicant's amendments to the claims necessitated the foregoing new grounds of rejection. Although rendered moot by the foregoing new grounds of rejection, Applicant's arguments have been carefully reviewed. Those arguments are not persuasive for at least the following reasons.

Applicant argues:

The Office Action acknowledges that Ussery does not disclose "means for identifying bit demands" but points to Shackleford for remedying this deficiency. Applicant respectfully submits that the combination of Ussery and Shackleford does not render obvious that which is recited in claim 2, as amended.

Shackleford is directed to a processor synthesis system and a processor synthesis method for implementing an ASIC. (Col. 3, lines 6-8). Shackleford is directed to the problem of placing a CPU in an ASIC where the CPU is predefined with a bit width that may be more than is necessary. Using a larger than necessary CPU in an ASIC takes up additional room in the device. A CPU is synthesized that does not depend on a specific process technology and has the bit width customized to the requirements of the specific application. (Col. 3, lines 43-46). More specifically, the CPU bit

width is customized, "for example, when an 11-bit processor is required for a predetermined application, an 11-bit processor is synthesized instead of a 16-bit or 32-bit processor." (Col. 6, lines 50-57).

The cited combination, however, does not result in an application specific coprocessor system with a compiler that comprises "means for identifying bit demands,..such that each intermediate step in a calculation is allocated a minimal number of bits necessary" for producing a "final result that fulfills domain-specific objectives," as recited in claim 2, as amended. Applicant respectfully submits that Shackleford's teaching of customizing the CPU to the smallest bit width, in order to take up the least space in an ASIC, is not the same as allocating "a minimal number of bits necessary" for each "intermediate step," as recited above.

For at least the foregoing reason, Applicant respectfully submits that independent claim 2, and its dependent claims, are allowable over the cited combination of references.

Applicant respectfully submits that independent claim 8, and its dependent claims, are patentable over the cited combination of references for at least the same reasons as submitted above with respect to claim 2.

Applicant respectfully submits that independent claim 16 is patentable over the cited combination of references for at least the same reasons as submitted above with respect to claim 2.

Applicant respectfully submits that independent claim 21, and its dependent claims, are patentable over the cited combination of references for at least the same reasons as submitted above with respect to claim 2.

Applicant respectfully submits that independent claim 30 is patentable over the cited combination of references for at least the same reasons as submitted above with respect to claim 2.

Examiner respectfully disagrees. Firstly, "each intermediate step" in the claims may be allocated the same bit width, *i.e.*, the "minimal number of bits necessary for producing a final result that fulfills domain-specific objectives," within the limits of the claim. Ussery and Shackleford disclose this limitation, as Applicant's arguments appear to admit. Secondly, even if "each intermediate step" could be allocated a different bit width, which is *not* supported, or at least not clearly supported, by the specification, the

structure of the amended claims does not require any further calculation or allocation of bit width once the "minimal number of bits necessary for producing a final result that fulfills domain-specific objectives" is identified. Once again, Ussery and Shackleford disclose the computation of a bit width in accordance with the foregoing interpretations of the contested claim limitation. Accordingly, Applicant's arguments in traversal of the art rejections are not persuasive, and all pending claims stand rejected as set forth above.

Conclusion

Applicant's amendment necessitated any new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to RYAN D. COYER whose telephone number is (571) 270-5306 and whose fax number is (571) 270-6306. The examiner normally can be reached via phone on Mon-Thurs, 7a-6p. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Li B. Zhen, can be reached on (571) 272-3768. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ryan D. Coyer/
Examiner, Art Unit 2197

/Li B. Zhen/
Supervisory Patent Examiner, Art Unit 2197